Enhancement mode GaAs PHEMT LNA with linearity Control (IP3) and Phased matched Mitigated Bypass Switch and Differential Active Mixer

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Abstract — A new Front End IC has been designed using single supply enhancement mode GaAs PHEMT 0.5 μm process for WCDMA and other wireless application. This Front End has single ended LNA, single ended in & differential out active balanced mixer with integrated LO active balun and buffer amplifier. The LNA also has CMOS logic controllable linearity (IP3) control and phased matched mitigated bypass switch. LNA draws 8.5mA current when switched to high linearity mode and has 15dB gain, 1 dB NF, -6 dBm IP_{1dB} and 7.3dBm IIP3. In low linearity mode it draws 3.5mA current and has 14dB gain, 1.1 dB NF, -6 dBm IP_{1dB} and 2 dBm IIP3. In LNA bypass mode total bypass loss is <3.5 dB and has 7 dB NF, 5 dBm IIP3 and it draws ~1mA current. Also the bypass switch circuit has an integrated active phase shift network which maintains the phase difference of <25° with LNA ON modes. In all condition LNA/switch combo has >10 dB I/O return loss. The Mixer with active balun and buffer amplifier consumes 8mA current and has 12dB gain, 7dB noise figure, 0dBm IIP3 and provides differential IF out with differential impedance of about 1000 ohms. Above performance is measured at 2.14 GHz for WCDMA application.

I. Introduction

Today's wireless communication receivers demand a low current consumption circuit with high RF performance with easy digital interface capability. This has generated a need for high performance device with simple single bias capability. Normally this is easily doable in Si /SiGe based devices but conventional depletion mode GaAs devices lack it. In order to cope this problem a very few GaAs based foundries have been able to develop enhancement mode GaAs devices which operates very similar to BJT but have better noise figure, power and linearity. Also such devices have easy capability to do digital controllable switches due to its switch like operation and single polarity supply requirement.

Fig. 1 shows a typical wireless transceiver of a portable device. In order to get better performance from portable devices, there is a need to sense the incoming signal strength and make the transceiver circuits to respond accordingly. This also helps to prolong battery usage as current consumption varies, which is a very important consideration for any handset or a portable device. The circuits mentioned in this paper address both the issues. This paper discusses the design of **LNA** integrated with **mitigated bypass switch** containing an **active phase shift element** in its bypass switch path and a very low current **active balanced Mixer** with **active balun** and **single ended in / differential out LO buffer amplifier.**

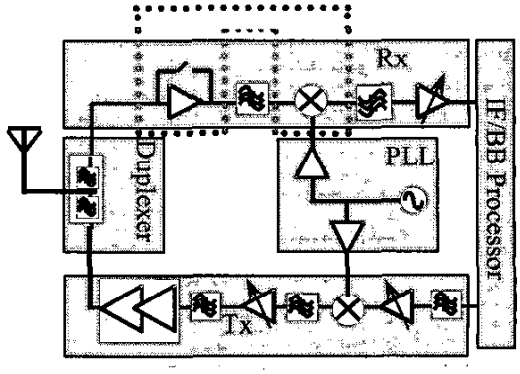

Fig. (1): Typical Wireless Transceiver

The designed LNA operates in three different signal strength zones (i) strong signal strength zone, (ii) moderate signal strength zone (iii) Weak signal strength zone. When the transceiver is close to base station, signal strength is very high, in this case there is no amplification of incoming signal is required and so transceiver's LNA is turned OFF and its bypass (**BP**) mitigated switch is turns ON (in typical urban area, 80% of the time handsets or any portable device operate in this zone). This help to maintain receiver chain linearity and power handling capability and also LNA consumes minimum current ~1mA. When the transceiver is far away from base station, signal strength is very weak. In this situation receiver of the Transceiver

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needs maximum amplification of input signal with minimum noise figure and also requires high linearity (**HL**), as transmitter power leakage is significant in the receiver. The LNA in this case provides maximum gain, minimum noise figure, highest P_{1dB} & linearity and consumes maximum current. In the medium signal strength zone, LNA turns ON in low linearity (**LL**) mode and operates at less than half current of HL modes and gives a little lower performance than HL mode. This way LNA saves a lot of current and prolongs battery life also helps to maintain optimum RF operating condition for the subsequent circuits of the transceiver.

The LNA-Switch operates between duplexer and an image reject filter. It is therefore important for LNA-Switch should provide decent match to these elements otherwise there will be significant gain ripple in the signal pass band and/or filter shift response shift which would degrade the system performance. To minimize this Mitigation circuit has been has been designed in the switch path. This circuit helps the switch path to maintain I/O impedance close to LNA's I/O impedance and thus avoids any mismatch between two states and a simple L, C match can provide a decent match at any frequency of interest for all modes. There is another problem in the Switch state is that it provides 0° S21 phase shift and LNA provides 180° S21 phase shift. This may cause data frame lost and not acceptable for some application. To overcome this problem, a unique active, ultra low current phase shift element has been added in the Switch path without any significant loss in its linearity. Previous reported [1-4] LNA/Bypass switch was designed using depletion mode PHEMT process had high loss with external current setting element. This design is based on enhancement mode PHEMT process and has very low loss broadband mitigated bypass digital controllable switch with active S21 phase shift circuits. It also has digitally controllable IP3 switch.

Another limitation of GaAs devices is, it has low transconductance compared to Si/SiGe based devices. This make the Mixer design difficult for low LO power operation. The problem further complicates if it has to be driven differentially, because it needs a really high LO drive power for proper operation of mixer. This paper discusses design technique of a low LO power Mixer with unique very low current LO buffer amplifier. The performance of this mixer is better than comparable Si/SiGe based mixer and it consumes a little lower power too.

II. Circuit Design

Top level schematic of LNA + Mixer is shown in fig. (2). The designs consist of a LNA with mitigated bypass switch and an integrated transmission (S21) phase shift element in its bypass path. Different LNA modes and Switch phase shift can be digitally controlled using a external logic. Two versions of this LNA has been design for 0/3V & 3/0V logic. Schematic of LNA alone is

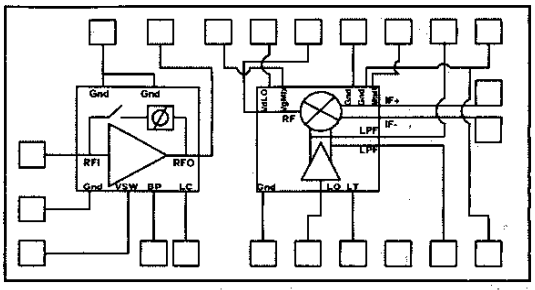

Fig. (2): Top level schematic of Front End IC

shown in fig. (3). The authors in previous work [5] have reported the functionality of similar LNA. The new added feature is very low current, low loss switch with phase shift element without sacrifice of switch IP3. This has been done with the help of Mitigator and IP3 control circuit shown in fig. (3). Schematic of Mixer, Active Balun with Buffer Amplifier is shown in Fig. (4). Mixer is very similar to half Gillbert cell and has a linearity control port in the tail of tranconductance FET. This helps to increase mixer linearity externally. A LC tank circuit has been added at the differential IF ports to suppress the LO & RF leakage. The current consumption of the mixer is 6mA. The LO section of the mixer draws about 2mA current. It is consist of single ended to differential out active balun with high voltage gain differential buffer amplifier. The output impedance of a conventional differential amplifier is sensitive to its DC operating current. When the current is very low as in the case of this work, its output impedance is very high. When these high impedance output ports feed the gates of the mixing devices, it causes significant amount of RF voltage drop. The reason for this drop is gate impedance of mixing device is lower than the output of the LO differential amplifier. In order to overcome this difficulty an impedance invertor common drain pair has been added to the output of the differential amplifier. This impedance invertor brings the output of the differential pair to very low value and when this pair feeds the gates of mixing FET, RF voltage is almost doubled as gate impedance of mixing devices is much higher than the impedance of this

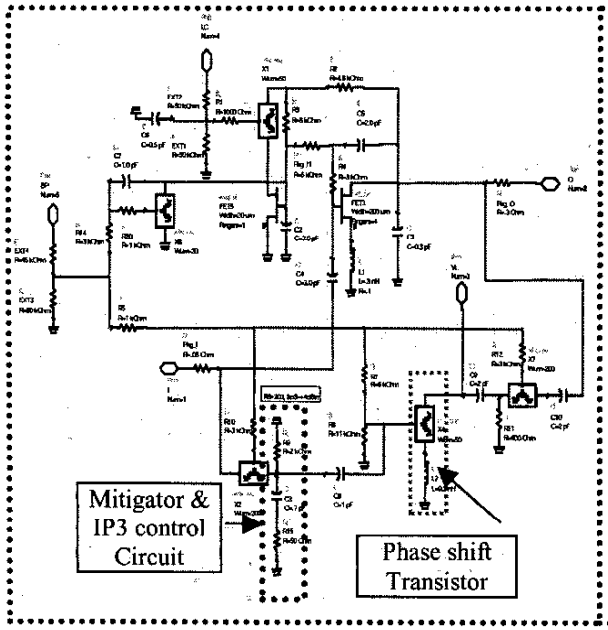

Fig. (3): LNA/Mitigated Bypass Switch schematic for 0/3V logic

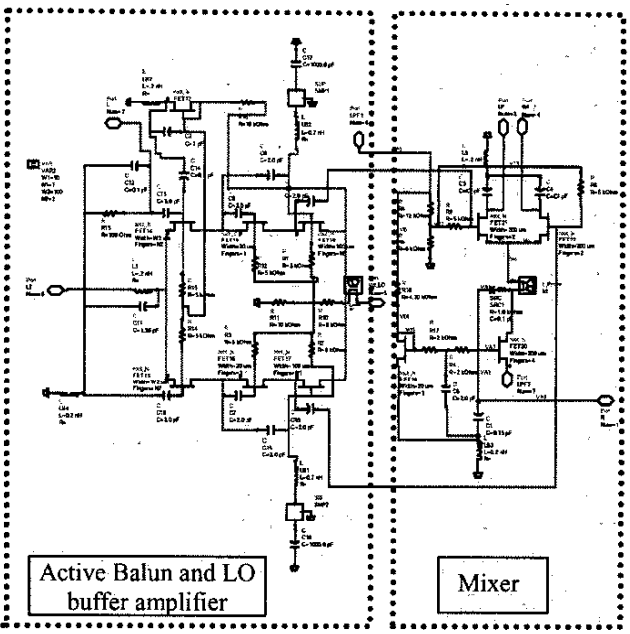

Fig. (4): Schematic of total Mixer circuit

pair. This technique makes this mixer to operate at very low LO power. Normally, noise figure of active mixer with integrated buffer amplifier tends to be very high, since there is no place to put an on *chip band pass filter* between amplifier and mixer due to component size constraints. In order to minimize IF noise feed-thru to the mixer from LO buffer amplifier, a high pass/low pass topology has been used. There is a low pass trap at the output of the differential amplifier, this shunts out the IF amplified noise from the buffer amplifier and send clean signal to the gates of mixing FET. This helps to bring the noise figure of the mixer close to the noise with the external band pass filter. The photograph of fabricated chip is shown in fig. (5).

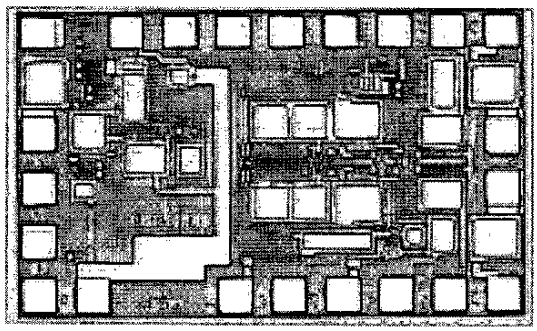

Fig. (5): Photograph of the fabricated IC

III. Measured Performance

Measured performance of the amplifier is shown in fig. (6a-d). Performance of the mixer is shown in fig. (7a-b). Cascaded LNA + Mixer performance is shown in fig. (8).

IV. Conclusion

An enhancement mode GaAs PHEMT based low noise, high gain front end has been developed with a few new features like low loss mitigated bypass switch with matched transmission phase in all modes of operation. The mixer of the front end requires very low LO power and performs better than comparable Si/SiGe based mixers with similar dc current consumption. A new topology has been used in LO buffer amplifier of the mixer to get high gain and low impedance out from it.

Reference

[1.] H. Morkner et. al., "An integrated FBAR and PHEMT Switched-AMP for wireless Applications.", IEEE, MTT-S, June 1999.

[2.] H. Morkner et. al., "A miniature PHEMT Switched –LNA for 800MHz to 8GHz Handset application.", RFIC, June 1999.

[3.] Ray Moroney et. al., "A high performance Switch-LNA IC for CDMA handset receiver applications.", RFIC, June 1995.

[4.] Patent: H. Morkner, Mike Frank, "An Amplifier/Switch topology for Microwave application", 8 claims.

[5.] S. Kumar et. al., "Enhancement mode PHEMT LNA with LNA Linearity control and mitigated Bypass Switch.", RFIC, June 2002.

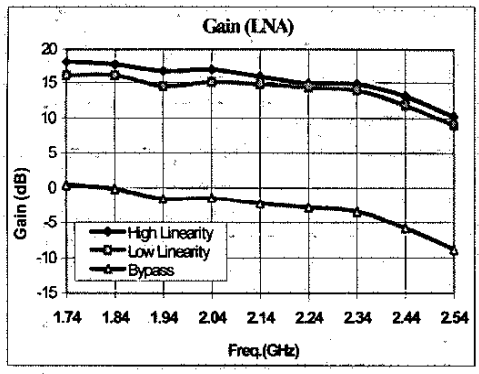

Fig. (6a) Measured gain of LNA in diff. mode

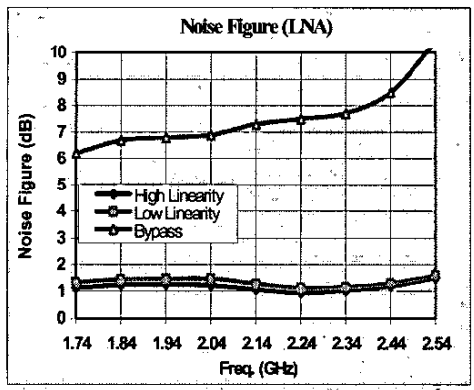

Fig. (6b) Measured NF of LNA in diff. mode

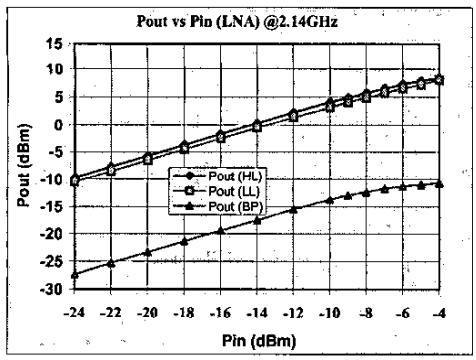

Fig. (6c) Pin Vs Pout of LNA in diff. mode

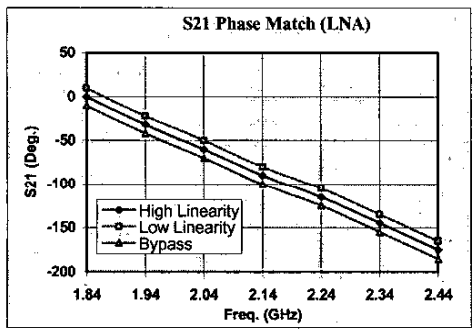

Fig. (6d) S21 phase of LNA in diff. mode

- Other LNA performance;
- I/O Return Loss > 10dB (All modes)
- Isolation > 20dB (All modes)
- IIP3 : 7.3dBm (HL)
  2.7dBm (LL)
  5.3dBm (BP)
- Vd=3.0V, Id=8.5mA (HL),
  3.5mA (LL), ~1mA (BP)

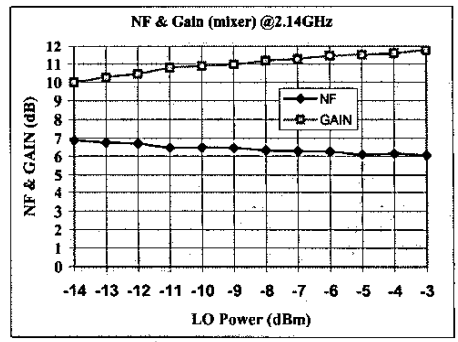

Fig. (7a) Measured NF & Gain of Mixer

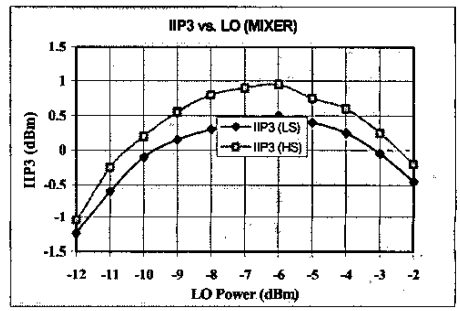

Fig. (7b) Measured IIP3 of Mixer

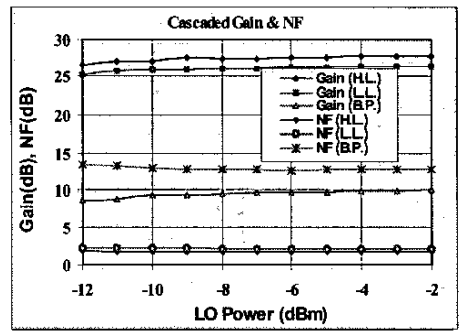

Fig. (8) Measured cascaded NF & Gain of LNA + Mixer using external IRF